Indian Journal of Electronics and Electrical Engineering (IJEEE)
Vol.2.No.2 2014pp 54-58
available at: www.goniv.com
Paper Received :15-04-2014
Paper Published:25-04-2014
Paper Reviewed by: 1. John Arhter 2. Hendry Goyal
Editor : Prof. P.Muthukumar

MINIMIZATION OF SWITCHING ACTIVITIES OF PARTIAL PRODUCTS FOR DESIGNING LOW POWER BAUGH WOOLLEY MULTIPLIER USING OPTIMIZED ADDER CELL

B.M.Prabhu,
Assitant Professor,
Angel College of Engineering and Technology,
Tirupur, India
bmprabhu16@gmail.com

Dr.S. Padma
Professor,
Sona College of Technology, Salem, India
swanisha@gmail.com

ABSTRACT

This article presents the design of multiplier. It means to perform a repeated addition while processing the addition we can get a multiplier and the performance of any processor or controller will depend upon its power, size and delay. So the power, size and delay should be less in order to get an effective processor or controller. Each and every processor has ALU (Arithmetic logic units). That arithmetic operation includes Addition, Subtraction, Multiplication, Division, shifter and many units. Multiplication is an important function in arithmetic operations, and it is more complex to develop the next level of bits. To illustrate the proposed multipliers exhibiting low power dissipation, the theoretical analyzing switching activates of partial products are derived and it is also used in DSP, multiplication process is used in many application like measurements and instrumentation applications such as filters, communication, Image processing, Robotics, Intelligence of embedded systems, special effects and graphics etc., The multiplier circuits are schematized and their layouts are design and generated by using VLSI CAD tools.

Key words: adder, multipliers, power consumptions and switching activities.

I. INTRODUCTION

BY increasing the demand on having, microprocessor and microcontroller with high speed and low power, designers should meet lot of problems In fact half adder is the most frequently used in processor for need of doing operation like adder, subtract, multiply and divide. To getting a various operation in ALU in such a wise of list multiplier unit is one of major units, with the highest level of power consumption and lowest speed. The multiplier is a basic building block in processor and controller. Multipliers having wide application in recent trends of embedded world. Multiplier is the processing of adding a number of partial products. It can be perform incisively mentioned that if speed, size and power of this multiplier unit is optimized, when the whole system can optimized in speed, size and power. For optimizing the partial product in those parameters, in the design of digital calculation systems, many units are applied.

Now the embedded world everywhere needs this technique for its size, speed and power are consumed.

Multiplier is performed an operation like a repeated addition so such additions are in digital electronic technique by full adder and half adder. The difference between full adder and half adder is that in half adder there is no input carry. For designing multiplier unit, which frequently is used in processing DSP, adder unit is used. But in some part of portion in partial product of multiplier unit half adder can also be used instead of full adder, because in comparison to full adder, half adder has low power consumption power and it perform a high speed, Because of by the reason the fewer number of transistor only used. In the operation of planner MOSFET scaling down of CMOS technology leads severe short channel effects will lead to degrade the performance. In designing digital integrated systems, occupied space, that is the number of transistor, are of high importance for designer. The lowest space is occupied by units, the best integration process can be done and make as a good result systems with higher speed and lower power can be designed.

II. CMOS BASED MULTIPLIER

CMOS based multiplier is existing method by based on Boolean method. Here the Shannon based logic adder is used to get reduce the number of transistor in CMOS and the power, size also be reduced.

While if we can reduce the number of transistor in adder means we can also implement in multiplier, regarding to design an 8x8 multiplier using by a Shannon full adder based, Unless taking the power consumption is dramatically reduced, the result will get a best processor package and performance of VLSI circuits and systems.

III. SHANNON FULL ADDER

The Shannon full Adder circuit as shown in fig.1 this Shannon adder operation that has sum and carry circuits are designed based on standard full adder equations.

In EX-OR gate portion can get result of sum and the processed AND gate based OR gated based to get result of carry. According to standard full adder equation, the sum circuits need three inputs. In order to avoid increasing the number of transistors due to addition of a third input, as the method of Shannon based adder is performed.

Shannon's Theorem

$$Carry = (A.B) + (B.B')$$

Shannon's full adder

$$Sum = ((A \text{ xor } B).C') + ((A \text{ xor } B)'.C)$$
$$Carry = ((A \text{ xor } B).C) + ((A \text{ xor } B)'.A)$$

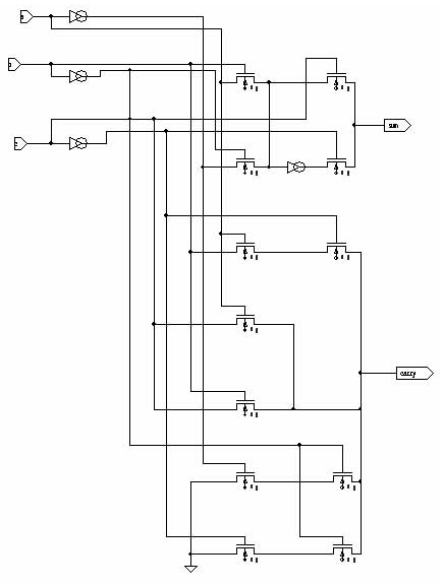

Fig.1.Shannon's adder cell

The number of bit multi operand addition can be extended to an n bit multi operand addition by cascading the carry save adder operation. The multiplier is schematized by Tanner s-edit power optimized multiplier using Shannon Based multiplier logic.

We have analyzed the basic circuits compared with Shannon adder based multiplier circuits in terms of power dissipation and area and observed better performance in my proposed Shannon based multiplier logic circuit. In a 20µm range based used in tanner tool and to reduce the transistor, speed of switching product increased by this Shannon's based adder.

This is possible to get a better result of taking size is optimized and it's reduced compare with normal CMOS adder, in this circuit, there is comparative reduction in the number of transistor and so reduction Area and power.

As per the normal full adder's table shown in Table.1

Table.1 Truth table of full adder

A	B	C	SUM	CARRY
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

IV. MODIFIED SHONNON BASED FULL ADDER CELL

The proposed Shannon full adder cells are based on The Shannon Theorem for the sum and carry operations. The full adder sum and carry circuits are designed based on standard adder circuit equations.

$$S = ABC + A'B'C + AB'C' + A'BC'$$
$$C = (A \oplus B)'B + (A \oplus B)\,C$$

Input B and its complement are used as the control signal for the sum circuit. The two input XOR gate is developed using the multiplexer method.

The output node of the two input multiplexer circuits is the differential node. According to standard full adder equation, the sum circuit needs three inputs. In order to avoid increase in number of transistors due to the addition of a third input, the following arrangement is made, the CPL X-OR gate multiplying with C's complement input and EX-NOR gate multiplying with input C, and thereby reducing the number of transistors in sum circuit. Comparing with previous circuit, this arrangement will increase the number of transistors but it avoid the critical path delay. The C and C' output nodes are called as differential node of the circuit for sun operation.

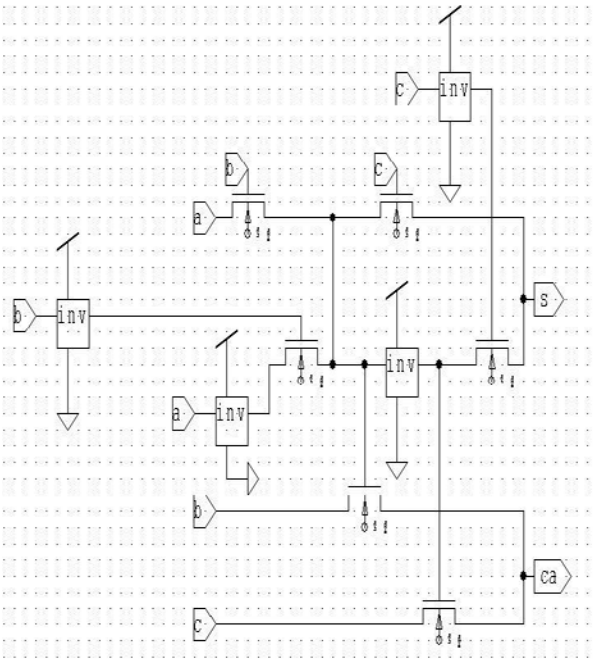

Fig.2. Modified Shannon adder cell

For carry operation A, B and their complements are used as a control inputs. A XOR B and its complement output node is called the differential node of the circuit for carry operation.

V. MULTIPLIER DESGIN

In this paper, we have going to propose a modified Shannon adder based multiplier here completely using by this multiplier when we have designed and analyzed carry save adder (CSA) multiplier circuit using based on Shannon's adder cell. The designed feature size is 20µm and corresponding supply voltage is 5v. And then various voltages based shown in table of content.

The carry save multiplier is a linear array multiplier as shown in Fig.2. The linear multiplier propagates data down through the array cell. Each row of CSAs adds one additional partial product to the partial sum. As the operand size increases, linear array grow at a rate equal to the square of the operand size because the number of rows in the array is equal to the length of the multiplier, and the width of each row is equal to the width of the multiplicand. By here we have shown in the Fig.2. 4*4 multiplier by using Shannon adder-based multipliers as it similar same to 8*8, 16*16 and 32*32 etc. here we shown tabulation as 8 bit multiplier and it has executed by low power consumption compared with normal gates based adder cell.

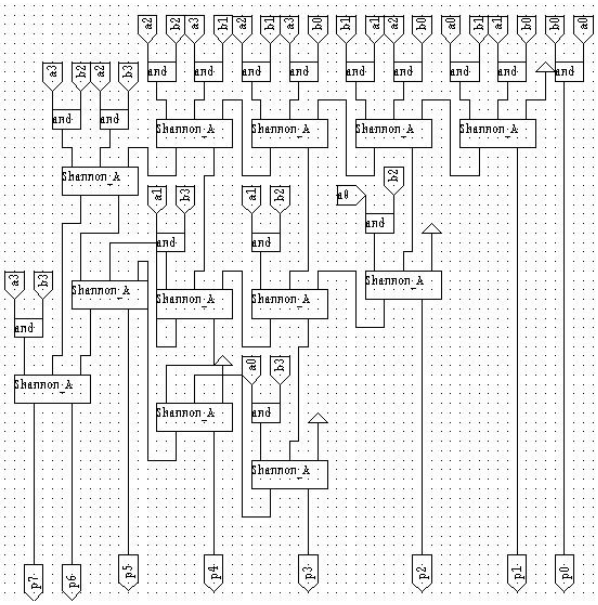

Fig.3. 4*4 Multiplier

VI. RELATED WORK

Adders operation performed with multipliers, one of the main reasons causing the leakage power increase of sub-threshold leakage power. When technology is developed to make a design to reduce the size through in nanometer range it will take by the power less module. And power calculation using Tanner tool s-edit

Tanner is used for schematic and output waveforms are observed. Propagation delay and area are calculated by using Tanner tool.

VII. RESULT AND DISCUSSION

In the multiplier array, a full adder with balanced carry and sum delays is desirable because the sum and carry signals are in the critical path. The speed and power of the full adder are very important for large arrays. The 8x8 bit multiplier circuits were simulated with a BSIM4 layout model. We compared the simulated results of our proposed 1-bit adder cell with existing author's results which shows better performance in terms of power dissipation and area. Our proposed 1-bit adder cell consumes less power, and less area than the various proposed 1-bit adder cells, due to regular arrangement of transistor tree structure, less critical path and multiplexing method of designs. The main reason for the lower propagation delay of Shannon-based multipliers is that they are balanced in the carry circuits. From the simulated results it is clear that the multiplier circuits designed based on the proposed adder cell gives better performance in terms of power, area than the CPL-based adder cell.

TABLE.2. SHANNON'S ADDER BASED OPERATING WITH 5.0 VOLT MULTIPLIER

S.no	Adder	Input bits	Power (mW)	Transistor count	Area μm^2	Speed (Ghz)	Delay (ns)	PDP(10^{-12} W-s)
1	Shannon Adder	8*8 Array Multiplier	0.0663	1,168	0.051392	13.39	74.65	4.94
2	Shannon Adder	8*8 Baugh wooley Multiplier	0.013	1,114	0.049016	114.54	8.73	0.11

TABLE.3. SHANNON'S ADDER BASED OPERATING WITH 3.0 VOLT MULTIPLIER

S.no	Adder	Input bits	Power (mW)	Transistor count	Area μm^2	Speed (Ghz)	Delay (ns)	PDP(10^{-12} W-s)
1	Shannon Adder	8*8 Array Multiplier	202.6	1,168	0.051392	15.71	63.62	0.128
2	Shannon Adder	8*8 Baugh wooley Multiplier	248.6	1,114	0.049016	136.42	7.33	0.182

TABLE.4. SHANNON'S ADDER BASED OPERATING WITH 1.5 VOLT MULTIPLIER

S.no	Adder	Input bits	Power (mW)	Transistor count	Area μm^2	Speed (Ghz)	Delay (ns)	PDP(10^{-12} W-s)
1	Shannon Adder	8*8 Array Multiplier	202.3	1,168	0.051392	160.51	6.23	1.26
2	Shannon Adder	8*8 Baugh wooley Multiplier	0.050	1,114	0.049016	251.88	3.97	1.98

VIII.RESULT

Performance analysis of Shannon based adder is obtained using simulated output. Hence here worked with array multiplier and Baugh wooley multiplier by using an Shannon adder Here the various volt based we have shown the Table.2 as operating with 5 volt, Table.3 as operating with 3 volt and Table.4 operating with 1.5 volt performed an operation in multiplier by using modified Shannon's adder cell and then when we going to increase a power the switching activities are increased at similarly when we operate with 1.5v that means low power consumed operating multiplier is getting a better result so that is major role of operation in this multiplier It take an operation getting a low power and get perfect result is possible in Shannon based adder cell.

IX. CONCLUSION

The Shannon adder based Carry save adder multipliers circuits are simulated by using Tanner's s-edit VLSI CAD tools and Parameters values are analyzed by using same tool.

The circuits were compared with existing circuits. Shannon adder based multiplier gives better performance than existing circuits in term of power dissipation and Area. The proposed multiplier circuits can be used in the low power application of VLSI circuits.

X. FUTURE WORK

In this paper, power dissipation and area of the multiplier using the proposed adder cell is compared with other multipliers designed using existing adders and used in DSP, multiplication process is used in many application like measurements and instrumentation applications such as filters, communication, Image processing, Robotics, Intelligence of embedded systems, special effects and graphics etc., Further it can be used in applications such as FIR filter, FFT, Rank order filters where adders and multipliers plays a major role.

REFERENCE

[1] P.Karunakaran, S.Venkatraman, I.Hameen Shanavas, T.Kapilachander "Power Optimized Multiplier Using Shannon Based Multiplexing Logic" I.J. Intelligent Systems and Applications, 2012, 6, 39-45 June 2012.

[2] C.Senthilpari, K.Diwakar and Ajay Kumar Singh "Low Power and High Speed 8x8 Bit Multiplier Using Non-clocked Pass Transistor Logics" November 2009

[3] C.Senthilpari, K.Diwakar and Ajay Kumar Singh "High speed and High Throughput 8x8 Bit Multiplier using a Shannon –based Adder Cell" April 2009.

[4] Padmanabhan Balasubramanian and Nikos E. Mastorakis "High Speed Gate Level Synchronous Full Adder Designs" WSEAS Transactions on circuits and systems February 2009.

[5] Z. Abid, H. El-Razouk, D.A. El-Dib "Low power multipliers based on new hybrid full adders" Microelectronics. J (2008), doi: 10.1016/ j.mejo.2008.04.002.

[6] Reto Zimmermann and Wolfgang Fichtner "Low-Power Logic Styles: CMOS versus Pass- Transistor Logic" IEEE Journal of Solid-State Circuits, Vol.32, No.7, April 1997, pp.1079–1090.

[7] K. Navi, M.H Moaiyeri, R. F.Mirzaei, O. Hashemipour, B. M.Nezhad, Jan. (2009), "Two New LowPower Full Adder Based on majority-not Gates" Microelectronics Journal, Elsevier, vol. 40, no. 1, pp. 126-130.

[8] Melaka ,Malaysia,C.senthilpari,S.kavitha and jude joseph. "Lower Delay and Area Efficient Non-Restoring Array Divider by Using Shannon Based Adder Technique" ICSE 2010 Proc,2010.

[9] Reto Zimmermann and Wolfgang Fichter,Fellow, IEEE. "Low –Power Logic style:CMOS versus Pass-Transistor Logic" IEEE journal of solid – state circuits,july 1997.

[10] Iiham Hassoune ,denis flandre,Ian O'conner. And Jean Didier LEgat "ULPFA:A New Efficient Design of a Power-aware Full adder" IEEE Transcation on circuits and systems-august 2010.

[11] "Kiamal Z.pekmestzi" speed comparison of 16×16 Vedic Multiplier",internation journal of computer applications May 2011.

[12] Hajira Fathima, Jahangeer Md & Kaleem Fatima "Design of Low Power Shannon Based Adder cell using Multipliexing control Input Technique".

[13] Harshvardhan Upadhyay Comparsion and Abhishek Choubey "Comparison for leakage reduction in CMOS inverter with Stack keeper in VLSI design"